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Sample Solution for Problem Set 4
Due: May 15, 2007, 9:14 am

Embedded Systems

Problem 1 (Matlab/Stateflow)

Initial model (after exercise 1)

Your model should look similar to this after finishing the first exercise.

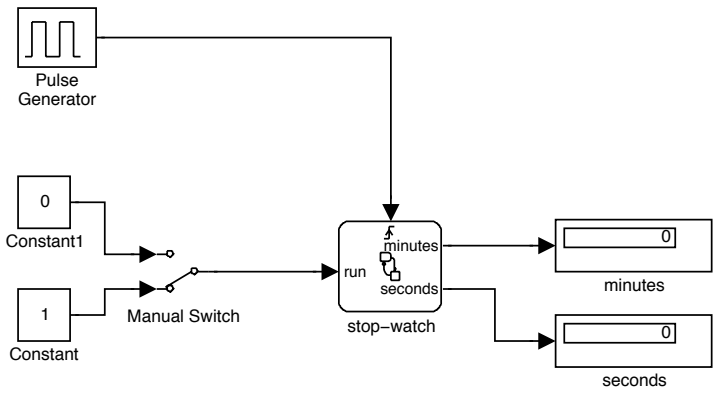

Figure 1: Initial model, simulink part

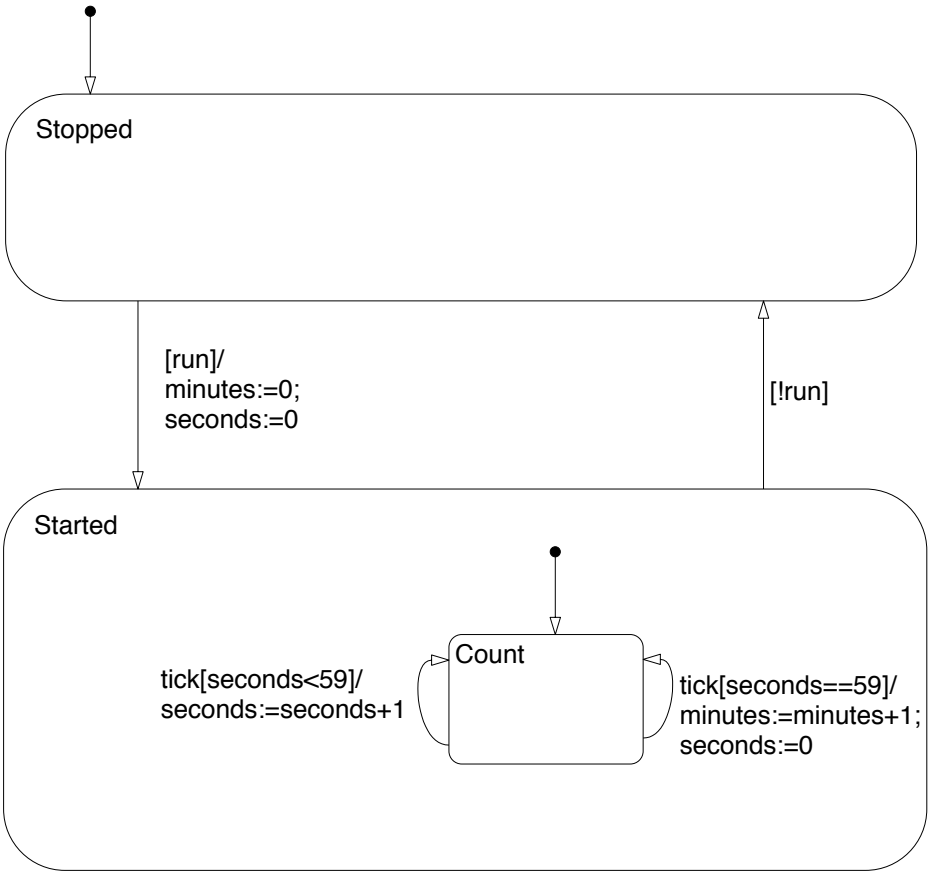

Figure 2: Initial model, stateflow part

Model after exercise 2.1

Here you should have added a switch for the lap. In the StateFlow model you need some technique to go on counting while not displaying anything. This has been done by having two variables for internal representation of seconds/minutes and for external representation of them.

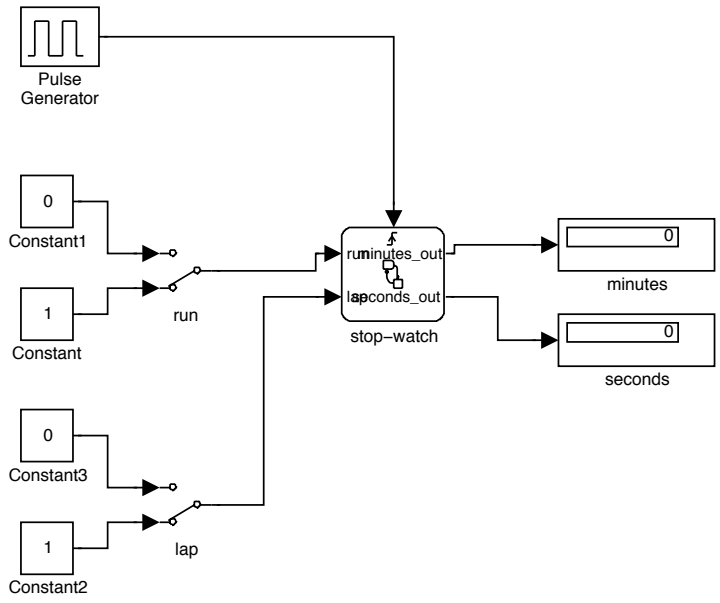

Figure 3: After exercise 2.1, simulink part

Model after exercise 2.2

We need an additional switch for the store/recall funtion. To model the store/recall functionality, the state “Memory” has been placed in parallel to the whole clock. In this state, variables “mem_seconds” and “mem_minutes” are written and read to store and recall the values of minutes and seconds respectively.
Notice that we use a connection junctor to enter the right state in the beginning.

Model after exercise 2.3

To change the reset functionality, the reset on the transition labelled with “[run]” is removed. Then, the store/recall state which lay in parallel to the whole clock is split into two parts where one goes to the part for the stopped and the other for the running clock. The part for the running clock is like the one of the previous exercise, whereas in the one for the stop state we model model the behaviour to reset the clock to zero.

Model after exercise 2.4

To increase the internal working speed of the clock, one has to increase the frequency of the clock by setting its period to 0.1. But then you must make shure to only increase time by a second each 10 ticks. This is done by the variable “tick_counter”. It is increase till it reaches 9 and then reset to 0. Each time it is 9, that is each second, we increase the time by one second.

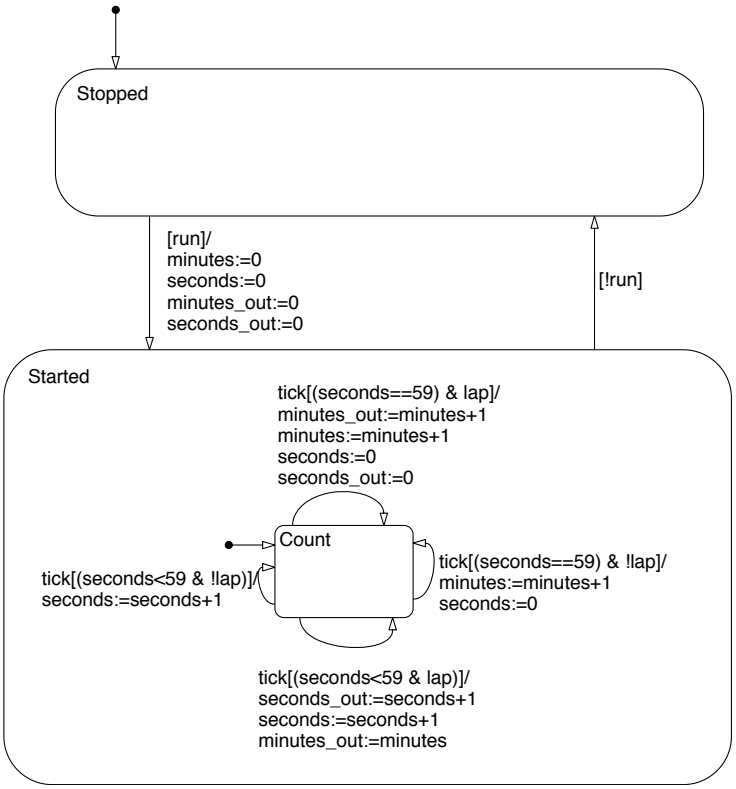

Figure 4: After exercise 2.1, stateflow part

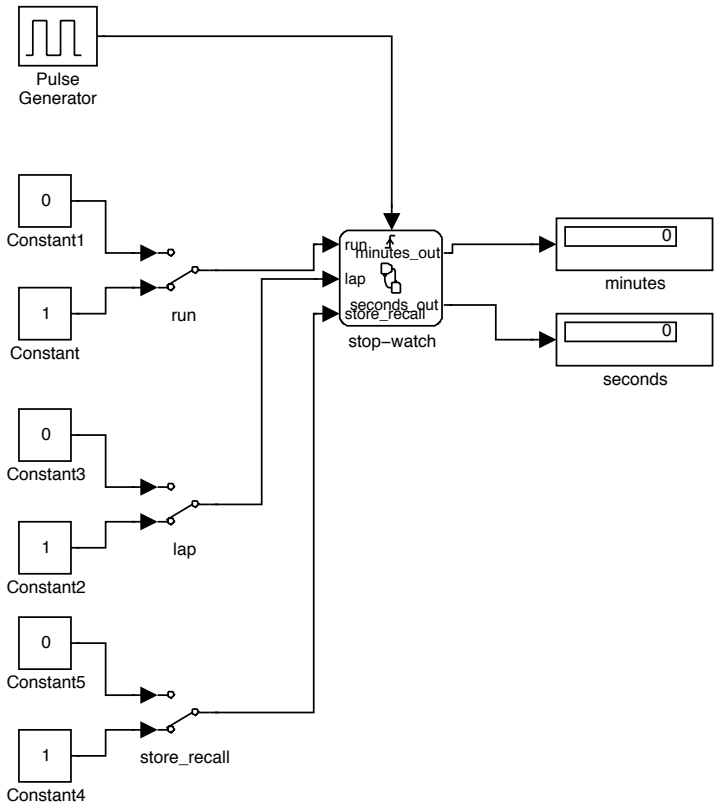

Figure 5: After exercise 2.2, simulink part

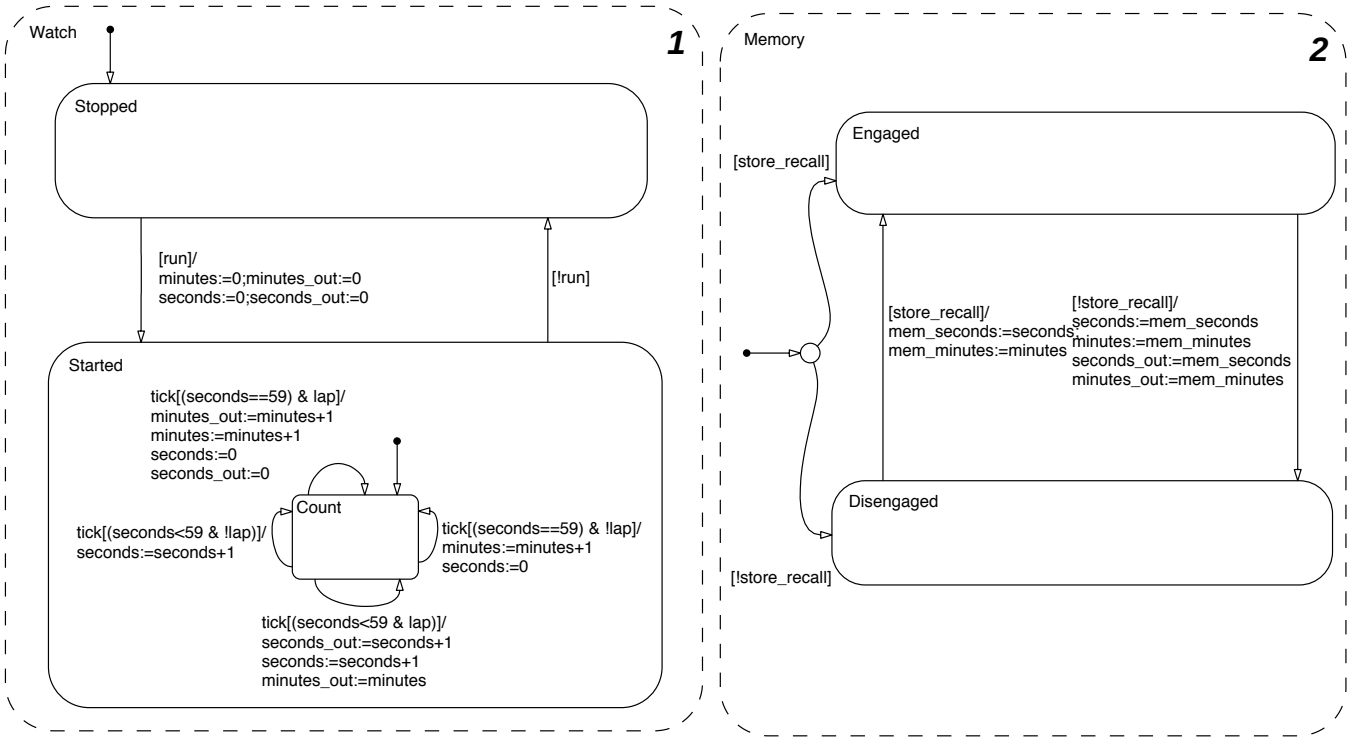

Figure 6: After exercise 2.2, stateflow part

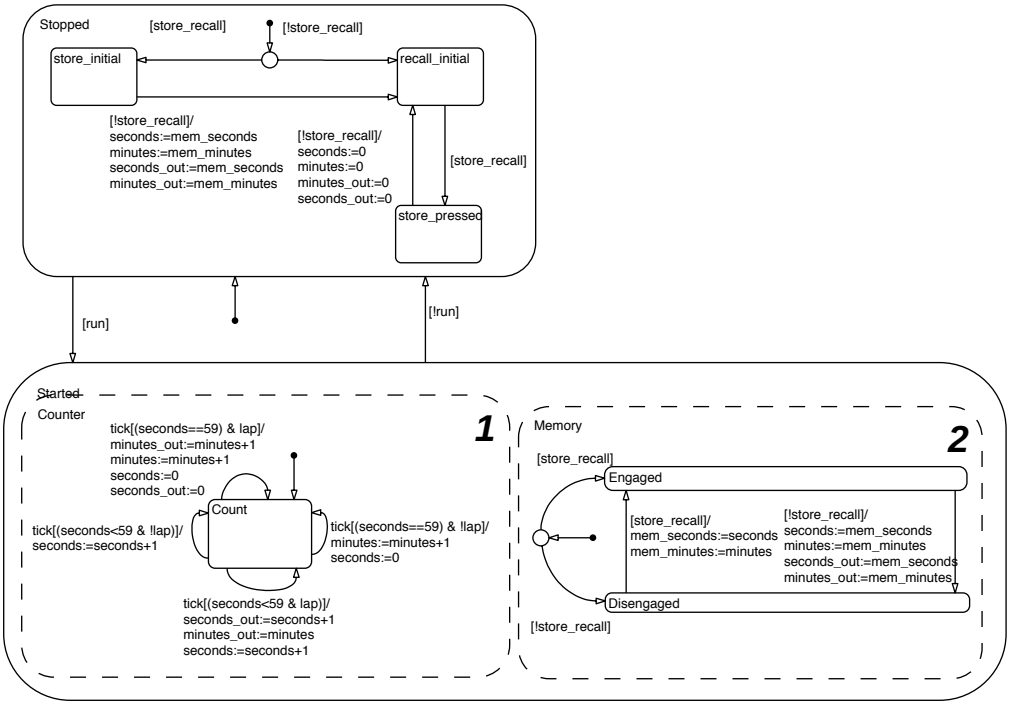

Figure 7: After exercise 2.3, stateflow part

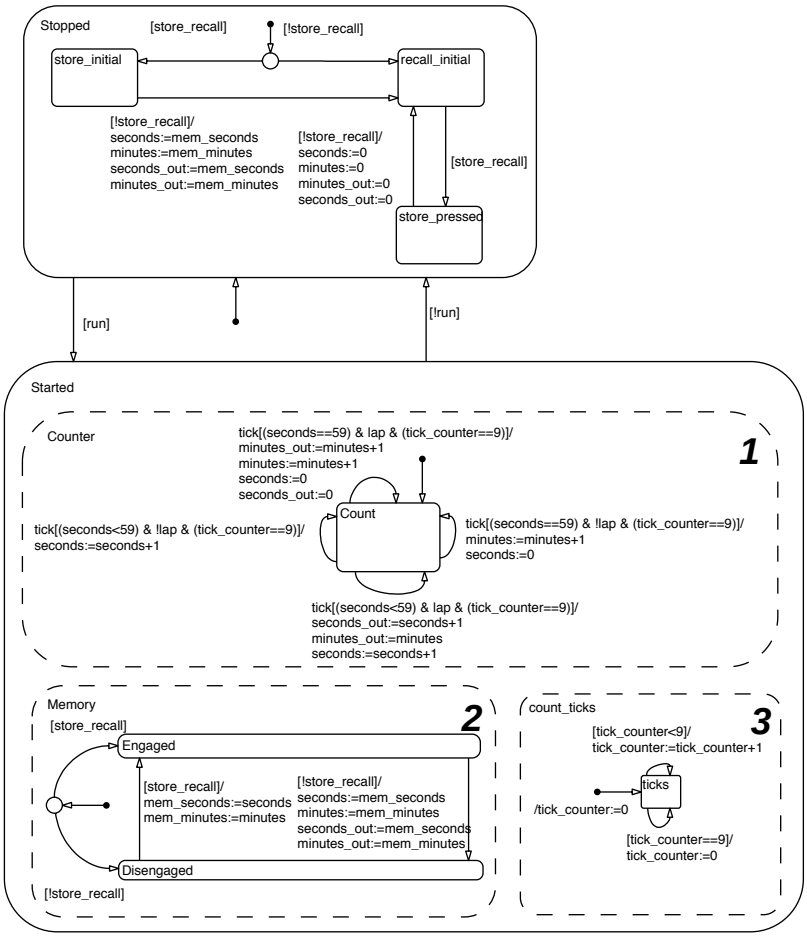

Figure 8: After exercise 2.4, stateflow part