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Problem Set 5
Due: June 12, 2007, 9:14 am

Embedded Systems

Problem 1 (VHDL) — 20 points

Write a *behavioral* and a *structural* architecture implementing a **multiplexer**. Start with the following declaration.

```
entity multiplexer is
   port(x, a, b: in Bit; h: out);
end multiplexer;
```

You must ensure that:

$$h = \begin{cases} a\,, & \text{if } x = 0\,, \\ b\,, & \text{if } x = 1\,. \end{cases}$$

When writing the structural architecture, you can use gates (NOT, AND, OR, NAND, NOR, XOR) as your starting subentities.

Problem 2 (VHDL) — 40 points

Write a *behavioral* and a *structural* architecture implementing a **4-bits adder**, as well a *behavioral* and a *structural* architecture implementing a **saturating 4-bits adder**. Start with the following declaration.

```
entity adder is
   port(a3, a2, a1, a0, b3, b2, b1, b0: in bit; c3, c2, c1, c0, d: out);
end adder;
```

Let

$$\begin{aligned} a &= 8a_3 + 4a_2 + 2a_1 + a_0\,, \\ b &= 8b_3 + 4b_2 + 2b_1 + b_0\,, \\ c &= 8c_3 + 4c_2 + 2c_1 + c_0\,. \end{aligned}$$

Denote with $+_{16}$ addition modulo 16. Denote with $+^s_{16}$ saturating addition modulo 16, that is:

$$a +^s_{16} b = \begin{cases} a + b\,, & \text{if } a + b \leq 15 \\ 15\,, & \text{otherwise}\,. \end{cases}$$

You must ensure that:

- $c = a +_{16} b$, for the 4-bits adder;
- $c = a +^s_{16} b$, for the saturating 4-bits adder;
- in all cases: $d = 1$ iff there was an overflow, i.e., $a + b > 15$.

When writing the structural architectures, you can use full adders, half adders, and gates as your starting subentities. *Full adders and half adders were described during the lecture.*

Problem 3 (VHDL) — 40 points

Write a *behavioral* and a *structural* architecture implementing a **4-bits multiplier**, as well a *behavioral* and a *structural* architecture implementing a **saturating 4-bits multiplier**. Start with the following declaration.

```
entity multiplier is
   port(a3, a2, a1, a0, b3, b2, b1, b0: in bit; c3, c2, c1, c0, d: out);
end multiplier;
```

Let

$$a = 8a_3 + 4a_2 + 2a_1 + a_0\,,$$
$$b = 8b_3 + 4b_2 + 2b_1 + b_0\,,$$
$$c = 8c_3 + 4c_2 + 2c_1 + c_0\,.$$

Denote with $*_{16}$ multiplication modulo 16. Denote with $*^s_{16}$ saturating multiplication modulo 16, that is:

$$a *^s_{16} b = \begin{cases} ab\,, & \text{if } ab \leq 15 \\ 15\,, & \text{otherwise}\,. \end{cases}$$

You must ensure that:

- $c = a *_{16} b$, for the 4-bits multiplier;
- $c = a *^s_{16} b$, for the saturating 4-bits multiplier;
- in all cases: $d = 1$ iff there was an overflow, i.e., $a + b > 15$.

When writing the structural architectures, you can use full adders, half adders, and gates as your starting subentities. You can also reuse any entity that you defined when solving Problem 2.